PATENT

Attorney's Docket No.: U 012239-9

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of Inventor:

MING-SHIEN **LEE**

WARNING: *The Declaration must name all of the actual inventor(s).*

For (title):
COMPUTER SYSTEM HAVING AN INTEGRATED CORE AND GRPAHIC CONTROLLER DEVICE CAPABLE OF ACCESSING MEMORY DATA SIMULTANEOUSLY FROM A SYSTEM MEMORY POOL AND A SEPARATE STAND-ALONE FRAME BUFFER MEMORY POOL

5/7/99

1. Type of Application

This new application is for a(n) (check one applicable item below):

- ☑ Original (nonprovisional)
- ☐ Design
- ☐ Plant

WARNING: ***Do not*** *use this transmittal for a completion in the U.S. of an International Application under 35 U.S.C. 371(c)(4) unless the International Application is being filed as a divisional, continuation or continuation-in-part application.*

WARNING: ***Do not*** *use this transmittal for the filing of a provisional application.*

CERTIFICATION UNDER 37 CFR 1.10

I hereby certify that this New Application Transmittal and the documents referred to as enclosed therein are being deposited with the United States Postal Service on this date **MAY 7, 1999 in an envelope as "Express Mail Post Office to Addressee" Mailing Label Number EE784098748US addressed to the: Assistant Commissioner of Patents, Washington, D.C. 20231**

GERALDINE MARTI
(type or print name of person mailing paper)

Geraldine Marti
(Signature of person mailing paper)

NOTE: ***Each paper or fee referred to as enclosed herein has the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 CFR 1.10(b).***

WARNING: ***Certificate of mailing (first class) or facsimile transmission procedures of 37 CFR 1.8 cannot be used to obtain a date of mailing or transmission for this correspondence.***

EE784098748US

2. Benefit of Prior U.S. Application(s) (35 U.S.C. 119(e), 120, or 121)

NOTE: If the new application being transmitted is a divisional, continuation or a continuation-in-part of a parent case, or where the parent case is an International Application which designated the U.S., or benefit of a prior provisional application is claimed, then check the following item and complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

WARNING: *If an application claims the benefit of the filing date of an earlier filed application under 35 U.S.C. 120, 121 or 365(c), the 20-year term of that application will be based upon the filing date of the earliest U.S. application that the application makes reference to under 35 U.S.C. 120, 121 or 365(c). (35 U.S.C. 154(a)(2) does not take into account, for the determination of the patent term, any application on which priority is claimed under 35 U.S.C. 119, 365(a) or 365(b).) For a c-i-p application, applicant should review whether any claim in the patent that will issue is supported by an earlier application and, if not, the applicant should consider canceling the reference to the earlier filed application. The term of a patent is not based on a claim-by-claim approach. See Notice of April 14, 1995, 60 Fed. Reg. 20,195, at 20,205.*

WARNING: *When the last day of pendency of a provisional application falls on a Saturday, Sunday, or Federal holiday within the District of Columbia, any nonprovisional application claiming benefit of the provisional* ***must*** *be filed prior to the Saturday, Sunday or Federal holiday within the District of Columbia. See 37 C.F.R. § 1.78(a)(3).*

☐ The new application being transmitted claims the benefit of prior U.S. application(s) and enclosed are ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

NOTE: If one of the following 3 items apply, then complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF A PRIOR U.S. APPLICATION CLAIMED and a NOTIFICATION IN PARENT APPLICATION OF THE FILING OF THIS CONTINUATION APPLICATION.

☐ Divisional.

☐ Continuation.

☐ Continuation-in-Part (C-I-P).

3. Papers Enclosed That Are Required For Filing Date Under 37 CFR 1.53 (Regular) or 37 CFR 1.153 (Design) Application

_9_ Pages of specification

_2_ Pages of claims

_1_ Pages of Abstract

_4_ Sheets of drawing

☑ formal

☐ informal

WARNING: ***DO NOT*** *submit original drawings. A high quality copy of the drawings should be supplied when filing a patent application. The drawings that are submitted to the Office must be on strong, white, smooth, and non-shiny paper and meet the standards according to § 1.84. If corrections to the drawings are necessary, they should be made to the original drawing and a high-quality copy of the corrected original drawing then submitted to the Office. Only one copy is required or desired. Comments on proposed new 37 CFR 1.84. Notice of March 9, 1988 (1990 O.G. 57-62).*

NOTE: "Identifying indicia, if provided, should include the application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application. This information should be placed on the back of each sheet of drawing a minimum distance of 1.5 cm. (⅝ inch) down from the top of the page." 37 C.F.R. 1.84(c).

(complete the following, if applicable)

☐ The enclosed drawing(s) are photograph(s), and there is also attached a "PETITION TO ACCEPT PHOTOGRAPH(S) AS DRAWING(S)". 37 C.F.R. 1.84(b).

4. **Additional papers enclosed**

- ☐ Preliminary Amendment
- ☐ Information Disclosure Statement (37 CFR 1.98)
- ☐ Form PTO-1449
- ☐ Citations
- ☐ Declaration of Biological Deposit
- ☐ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.
- ☐ Authorization of Attorney(s) to Accept and Follow Instructions from Representative
- ☐ Special Comments
- ☐ Other

5. **Declaration or oath**

- ☐ Enclosed

  executed by *(check **all** applicable boxes)*

  - ☐ inventor.
  - ☐ legal representative of inventor. 37 CFR 1.42 or 1.43
  - ☐ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.
    - ☐ This is the petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 is also attached. *See item 13 below for fee.*
- ☑ Not Enclosed.

WARNING: *Where the filing is a completion in the U.S. of an International Application but where a declaration is not available or where the completion of the U.S. application contains subject matter in addition to the International Application the application may be treated as a continuation or continuation-in-part, as the case may be, utilizing ADDED PAGE FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION CLAIMED.*

- ☑ Application is made by a person authorized under 37 CFR 1.41(c) on behalf of *all the above named inventor.* (The declaration or oath, along with the surcharge required by 37 CFR 1.16(e) can be filed subsequently).

NOTE: It is important that all the correct inventor(s) are named for filing under 37 CFR 1.41(c) and 1.53(b).

- ☐ Showing that the filing is authorized. *(Not required unless called into question. 37 CFR 1.41(d).)*

6. **Inventorship Statement**

WARNING: *If the named inventors are each not the inventors of all the claims an explanation, including the ownership of the various claims at the time the last claimed invention was made, should be submitted.*

The inventorship for all the claims in this application are:

- ☐ The same
- ☐ Not the same. An explanation, including the ownership of the various claims at the time the last claimed invention was made,

7. **Language**

NOTE: An application including a signed oath or declaration may be filed in a language other than English. A verified English translation of the non-English language application and the processing fee of $130.00 required by 37 CFR

1.17(k) is required to be filed with the application or within such time as may be set by the Office. 37 CFR 1.52(d).

NOTE: A non-English oath or declaration in the form provided or approved by the PTO need not be translated. 37 CFR 1.69(b).

☑ English

☐ non-English

☐ the attached translation is a verified translation. 37 CFR 1.52(d).

8. Assignment

☑ An assignment of the invention to SILICON INTEGRATED SYSTEMS CORP.

☐ is attached. A separate ☐ "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or ☐ FORM PTO 1595 is also attached.

☑ will follow.

NOTE: "If an assignment is submitted with a new application, send two separate letters—one for the application and one for the assignment." Notice of May 4, 1990 (1114 O.G. 77-78).

WARNING: *A newly executed "CERTIFICATE UNDER 37 CFR 3.73(b)" must be filed when a continuation-in-part application is filed by an assignee. Notice of April 30, 1993. 1150 O.G. 62-64.*

9. Certified Copy

Certified copy of application

Country	Appln. No.	Filed

from which priority is claimed

☐ is attached.

☐ will follow.

NOTE: The foreign application forming the basis for the claim for priority must be referred to in the oath or declaration. 37 CFR 1.55(a) and 1.63.

NOTE: This item is for any foreign priority for which the application being filed directly relates. If any parent U.S. application or International Application from which this application claims benefit under 35 U.S.C. 120 is itself entitled to priority from a prior foreign application then complete item 18 on the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

10. Fee Calculation (37 CFR 1.16)

A. ☑ Regular Application

Claims as Filed

Number Filed		Number Extra		Rate	Basic Fee 37 CFR 1.16(a) $760.00
Total Claims (37 CFR 1.16(c))	6 - 20 =	0	x $	18.00	
Independent Claims (37 CFR 1.16(b))	1 - 3 =	0	x $	78.00	
Multiple dependent claim(s), if any (37 CFR 1.16(d))			+ $	260.00	

☐ Amendment cancelling extra claims enclosed.

☐ Amendment deleting multiple-dependencies enclosed.

☐ Fee for extra claims is not being paid at this time.

NOTE: If the fees for extra claims are not paid on filing they must be paid or the claims cancelled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency. 37 CFR 1.16(d).

Filing Fee Calculation $

B. ☐ Design application ($310.00 — 37 CFR 1.16(f))

Filing Fee Calculation $

C. ☐ Plant application ($480.00 — 37 CFR 1.16(g))

Filing Fee Calculation $

11. Small Entity Statement(s)

☐ Verified Statement(s) that this is a filing by a small entity under 37 CFR 1.9 and 1.27 is(are) attached or has been filed.

Filing Fee Calculation (50% of **A**, **B** or **C** above) $

NOTE: Any excess of the full fee paid will be refunded if a verified statement and a refund request are filed within 2 months of the date of timely payment of a full fee. 37 CFR 1.28(a).

12. Request for International-Type Search (37 CFR 1.104(d)) *(Complete, if applicable)*

☐ Please prepare an international-type search report for this application at the time when national examination on the merits takes place.

13. Fee Payment Being Made At This Time

☑ Not Enclosed

☑ No filing fee is to be paid at this time. *(This and the surcharge required by 37 CFR 1.16(e) can be paid subsequently.)*

☐ Enclosed

☐ basic filing fee $

☐ Recording assignment
($40.00; 37 CFR 1.21(h)) (See attached "COVER SHEET FOR ASSIGNMENT ACCOMPANYING NEW APPLICATION.")

☐ Petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached.
($130.00; 37 CFR 1.47 and 1.17(h)) $

☐ For processing an application with a specification in a non-English language.
($130.00; 37 CFR 1.52(d) and 1.17(k)) $

☐ Processing and retention fee
($130.00; 37 CFR 1.53(d) and 1.21(l))

☐ Fee for international-type search report
($40.00; 37 CFR 1.21(e)). $

NOTE: 37 CFR 1.21(l) establishes a fee for processing and retaining any application which is abandoned for failing to complete the application pursuant to 37 CFR 1.53(d) and this, as well as the changes to 37 CFR 1.53 and 1.78, indicate that in order to obtain the benefit of a prior U.S. application, either the basic filing fee must be paid or the processing and retention fee of §1.21(l) must be paid within 1 year from notification under §53(d).

Total fees enclosed $

14. Method of Payment of Fees

☐ Check in the amount of $

☐ Charge Account No. 12-0425 in the amount of $

A duplicate of this transmittal is attached.

NOTE: Fees should be itemized in such a manner that it is clear for which purpose the fees are paid. 37 CFR 1.22(b).

15. Authorization to Charge Additional Fees

WARNING: *If no fees are to be paid on filing, the following items should <u>not</u> be completed.*

WARNING: *Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges, if extra claim charges are authorized.*

☐ The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 12-0425.

☐ 37 CFR 1.16(a), (f) or (g) (filing fees)

☐ 37 CFR 1.16(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 CFR 1.16(d)), it might be best not to authorize the PTO to charge additional claim fees, except possibly when dealing with amendments after final action.

☐ 37 CFR 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)

☐ 37 CFR 1.17 (application processing fees)

WARNING: *While 37 CFR 1.17(a), (b), (c) and (d) deal with extensions of time under §1.136(a), this authorization should be made only with the knowledge that: "Submission of the appropriate extension fee under 37 C.F.R. 1.136(a) is to no avail <u>unless</u> a request or petition for extension is filed." (Emphasis added). Notice of November 5,1985 (1060 O.G. 27)*

☐ 37 CFR 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 CFR 1.311(b))

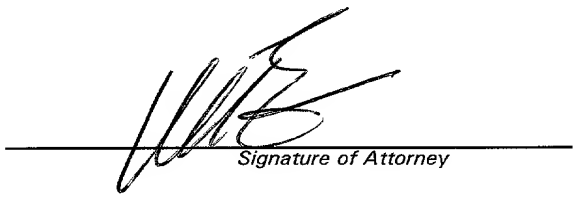
NOTE: Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of allowance. 37 CFR 1.311(b).

NOTE: 37 CFR 1.28(b) requires "Notification of any change in loss of entitlement to small entity status must be filed in the application ... prior to paying, or at the time of paying, ... issue fee". From the wording of 37 CFR 1.28(b): (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.

16. Instructions As To Overpayment

☐ credit Account No. 12-0425

☐ refund



Signature of Attorney

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☐ **Incorporation by reference of added pages**

(Check the following item if the application in this transmittal claims the benefit of prior U.S. application(s) (including an international application entering the U.S. stage as a continuation, divisional or C-I-P application) and complete and attach the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED)

☐ Plus Added Pages for New Application Transmittal Where Benefit of Prior U.S. Application(s) Claimed

Number of pages added ___

☐ Plus Added Pages for Papers Referred to in Item 4 Above

Number of pages added ___

☐ Plus "Assignment Cover Letter Accompanying New Application"

Number of pages added ___

☑ **Statement Where No Further Pages Added**

(If no further pages form a part of this Transmittal, then end this Transmittal with this page and check the following item:)

☑ This transmittal ends with this page.

U 012239-9

COMPUTER SYSTEM HAVING AN INTEGRATED CORE AND GRAPHIC CONTROLLER DEVICE CAPABLE OF ACCESSING MEMORY DATA SIMULTANEOUSLY FROM A SYSTEM MEMORY POOL AND A SEPARATE STAND-ALONE FRAME BUFFER MEMORY POOL

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to a computer system, more particularly to one having an integrated core and graphic controller device capable of accessing memory data simultaneously from a system memory pool and a separate stand-alone frame buffer memory pool.

2. Description of the Related Art

Referring to Figure 1, a conventional personal computer system 1 is shown to comprise a central processing unit (CPU) 10, a host bus 11 connected to the CPU 10, a core logic 12 connected to the host bus 11, a memory bus 13 connected to the core logic 12, a system memory pool 14 connected to the memory bus 13, an input/output (I/O) bus 15 connected to the core logic 12, at least one peripheral device 16 connected to the I/O bus 15, an Advanced Graphic Port (AGP) bus 17 connected to the core logic 12, a stand-alone graphic accelerator (VGA) card 18 connected to the AGP bus 17, and a monitor 19 connected to the VGA card 18. The VGA card 18 includes a VGA chip 181, a local frame buffer 182 formed from dynamic memory, and a flash memory 183 for VGA BIOS.

Referring to Figure 2, it has been proposed heretofore in another conventional personal computer system 2 to discard the stand-alone VGA card 18, and mount the VGA chip 181 and the local frame buffer 182 directly on the system board (not shown) to reduce costs and simplify manufacture of the system board.

Due to continued growth in multimedia applications, VGA processing needs more memory bandwidth and faster computing capability for larger data access to maintain optimum display quality and performance. Since the traditional VGA 64-bit frame buffer memory data (MD) bus cannot meet the performance target, a 128-bit frame buffer MD architecture has been proposed. The 128-bit MD bus lines allow the VGA chip to access 128-bit data per memory transaction to result in doubling of the performance as compared with the traditional 64-bit MD scheme. Figure 3 illustrates a proposed computer system 3 having a VGA chip 381 connected to a local frame buffer 383 via a 128-bit frame buffer MD bus 382. Although VGA performance is improved, too many memory pins are needed to make the proposed computer system 3 work. In a recommended memory signal layout on a system board, the layout trace width is about 6 mil, the spacing between traces is about 6 mil, the via hole diameter is about 12 mil, and the spacing between via is about 50 mil. Thus, for the proposed computer system 3, at least 6x64x2=768 mil is needed for the additional

64-bit MD signal lines, and more than 400 mil is spent for additional memory address and control signal lines. Therefore, the system board has to be enlarged to obtain sufficient trace space and for reasonable trace layout routing. This violates the trend toward making the system board more compact and more cost effective. In addition, the 128-bit MD bus lines will dramatically complicate the chipset-to-memory layout and will degrade the signal quality during run time. If BGA layout concerns are to be included, there is a need to reserve more space on the system board for extra signal pads or via holes. This further complicates the configuration of the system board and can cause heat distribution problems according to BGA design rules. Aside from the aforesaid disadvantages, in order to obtain the bandwidth benefit from the 128-bit MD bus lines in the proposed computer system 3, a two-bank graphic memory is needed to make the 128-bit MD bus lines feasible. This also violates the trend toward low-cost computer systems and high-density memory chips. In summary, too many pin counts not only result in an unacceptable increase in chip size, but also complicate the system board space/routing.

In co-pending U.S. Patent Application Serial Nos. 09/199,270 and 09/199,478, the applicant disclosed a computer system including an integrated core and graphic controller device that incorporates both core

logic controller and graphic controller functions, and a system memory that is shared by both the core logic controller portion and the graphic controller portion of the integrated core and graphic controller device, thereby achieving a unified memory architecture (UMA) that results in cost savings by reducing the system board space and the components on the system board. In addition, the system board space/routing effort and the memory bus pin counts are also minimized in the disclosed computer systems. However, if the 64-bit memory data bus is replaced by a 128-bit memory data bus in the disclosed computer systems to achieve better VGA performance, the problems of increased memory pin count and increased complexity of the system board space/routing will still be encountered.

SUMMARY OF THE INVENTION

Therefore, the object of the present invention is to provide an integrated core and graphic controller device capable of accessing memory data simultaneously from a system memory pool and a separate stand-alone frame buffer memory pool, whereby the benefit of more memory access bandwidth associated with 128-bit frame buffer memory data lines can be obtained for optimum graphical performance at the lowest memory pin count and without complicating the system board space/routing.

According to the present invention, a computer system comprises an integrated core and graphic controller device including a core logic controller portion and a graphic controller portion, a system memory pool, and a stand-alone frame buffer memory pool separate from the system memory pool. A first memory data bus interconnects the integrated core and graphic controller device and the system memory pool. A second memory data bus interconnects the integrated core and graphic controller device and the frame buffer memory pool. A memory address and control signal bus interconnects the integrated core and graphic controller device, the system memory pool and the frame buffer memory pool. The graphic controller portion of the integrated core and graphic controller device is capable of generating a same set of address signals received by the system memory pool and the frame buffer memory pool via the memory address and control signal bus such that the graphic controller portion is able to access simultaneously first word part display data from the system memory pool via the first memory data bus and second word part display data from the frame buffer memory pool via the second memory data bus.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the present invention will become apparent in the following detailed description of the preferred embodiment with

reference to the accompanying drawings, of which:

Figure 1 is a schematic circuit block diagram of a conventional personal computer system that incorporates a stand-alone VGA card;

Figure 2 is a schematic circuit block diagram of another conventional personal computer system that has a VGA chip and a local frame buffer mounted directly on a system board;

Figure 3 is a schematic circuit block diagram illustrating the conventional personal computer system of Figure 2 when modified to incorporate a 128-bit frame buffer memory data architecture; and

Figure 4 is a schematic circuit block diagram of the preferred embodiment of a computer system according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Figure 4, the preferred embodiment of a computer system 4 according to the present invention is shown to comprise a central processing unit (CPU) 40, a host bus 41 connected to the CPU 40, an integrated core and graphic controller device 42 connected to the host bus 41, a 64-bit quad-word first memory data bus 43 connected to the integrated core and graphic controller device 42, a system memory pool 44 connected to the first memory data bus 43, an input/output (I/O) bus 45 connected to the integrated core and graphic controller device 42, at least one peripheral device

46 connected to the I/O bus 45, a 64-bit quad-word second memory data bus 47 connected to the integrated core and graphic controller device 42, a stand-alone VGA-dedicated frame buffer memory pool 48 connected to the second memory data bus 47 and separate from the system memory pool 44, and a memory address and control signal bus 49 interconnecting the integrated core and graphic controller device 42, the system memory pool 44 and the frame buffer memory pool 48. Preferably, the system memory pool 44 is formed from standard DIMM, while the frame buffer memory pool 48 is formed from discrete DRAM chips.

The integrated core and graphic controller device 42 includes a core logic controller portion 421 and a VGA graphic controller portion 422. The architecture of the computer system 4 permits the graphic controller portion 422 of the integrated core and graphic controller device 42 to access the frame buffer memory pool 48 via the second memory data bus 47, and to share access to the system memory pool 44 with the core logic controller portion 421 via the first memory data bus 43. Particularly, during VGA processing, the graphic controller portion 422 generates a same set of address signals received by the system memory pool 44 and the frame buffer memory pool 48 via the memory address and control signal bus 49 such that the graphic controller portion 422 is able to access simultaneously low-

quad-word (64-bit MD) part display data from a lowest bank of the system memory pool 44 via the first memory data bus 43, and high-quad-word (64-bit MD) part display data from the frame buffer memory pool 48 via the second memory data bus 47. Thus, due to the presence of the two memory data bus 43, 47 that are connected to the two separate memory pools 44, 48, the integrated core and graphic controller device 42 can perform bi-quad-word (128-bit) memory data transactions without incurring an increase in memory pin count for each of the memory pools 44, 48.

As to how the graphic controller portion 422 shares access to the system memory pool 44 with the core logic controller portion 421, this can be done with the use of a built-in unified memory control unit (not shown) of the integrated core and graphic controller device 42, such as the ones described in the computer systems disclosed in co-pending U.S. Patent Application Serial Nos. 09/199,270 and 09/199,478 by the applicant.

Therefore, the computer system 4 of this invention provides the benefit of more memory access bandwidth associated with 128-bit frame buffer memory data lines for optimum graphical performance at the lowest memory pin count so that flexibility of system board space/routing can be ensured. Aside from using the same set of address signals to access the memory pools 44, 48 simultaneously during VGA processing, it is noted

that most of the control signals during memory access can also be shared by the memory pools 44, 48, thereby further reducing the size of the memory address and control signal bus 49. Furthermore, due to the presence of the VGA-dedicated frame buffer memory pool 48, the impact of a reduction in the size of the system memory pool 44, which is shared by both the core logic and graphic controller portions 421, 422, due to the use of a unified memory architecture can be minimized. As compared with the conventional computer systems of Figures 1 to 3, and the computer systems disclosed in the aforesaid co-pending U.S. patent applications, the computer system 4 of the present invention provides more flexibility in system board space/routing than the on-board VGA schemes utilized in the conventional computer systems of Figures 1 to 3, and more competitive VGA performance than the computer systems disclosed in the aforesaid co-pending U.S. patent applications. The object of the present invention is thus met.

While the present invention has been described in connection with what is considered the most practical and preferred embodiment, it is understood that this invention is not limited to the disclosed embodiment but is intended to cover various arrangements included within the spirit and scope of the broadest interpretation so as to encompass all such modifications and equivalent arrangements.

WHAT IS CLAIMED IS:

1. A computer system comprising:

an integrated core and graphic controller device including a core logic controller portion and a graphic controller portion;

a system memory pool;

a stand-alone frame buffer memory pool separate from said system memory pool;

a first memory data bus interconnecting said integrated core and graphic controller device and said system memory pool;

a second memory data bus interconnecting said integrated core and graphic controller device and said frame buffer memory pool; and

a memory address and control signal bus interconnecting said integrated core and graphic controller device, said system memory pool and said frame buffer memory pool;

said graphic controller portion of said integrated core and graphic controller device being capable of generating a same set of address signals received by said system memory pool and said frame buffer memory pool via said memory address and control signal bus such that said graphic controller portion is able to access simultaneously first word part display data from said system memory pool via said first memory data bus and second word part display data from said frame buffer

memory pool via said second memory data bus.

2. The computer system as claimed in Claim 1, wherein each of the first and second word part display data is a quad-word part data.

3. The computer system as claimed in Claim 2, wherein the first and second word part display data simultaneously accessed by said graphic controller portion from said system memory pool and said frame buffer memory pool form bi-quad-word display data.

4. The computer system as claimed in Claim 3, wherein each of the first and second word part display data includes 64 data bits.

5. The computer system as claimed in Claim 3, wherein the first word part display data is low word part display data, and the second word part data is high word part display data.

6. The computer system as claimed in Claim 1, wherein said system memory pool is formed from standard DIMM, and said frame buffer memory pool is formed from discrete memory chips.

ABSTRACT OF THE DISCLOSURE

A computer system includes an integrated core and graphic controller device having a core logic controller portion and a graphic controller portion, a system memory pool, and a stand-alone frame buffer memory pool separate from the system memory pool. A first memory data bus interconnects the integrated core and graphic controller device and the system memory pool. A second memory data bus interconnects the integrated core and graphic controller device and the frame buffer memory pool. A memory address and control signal bus interconnects the integrated core and graphic controller device, the system memory pool and the frame buffer memory pool. The graphic controller portion of the integrated core and graphic controller device generates a same set of address signals received by the system memory pool and the frame buffer memory pool via the memory address and control signal bus such that the graphic controller portion is able to access simultaneously first word part display data from the system memory pool via the first memory data bus and second word part display data from the frame buffer memory pool via the second memory data bus.

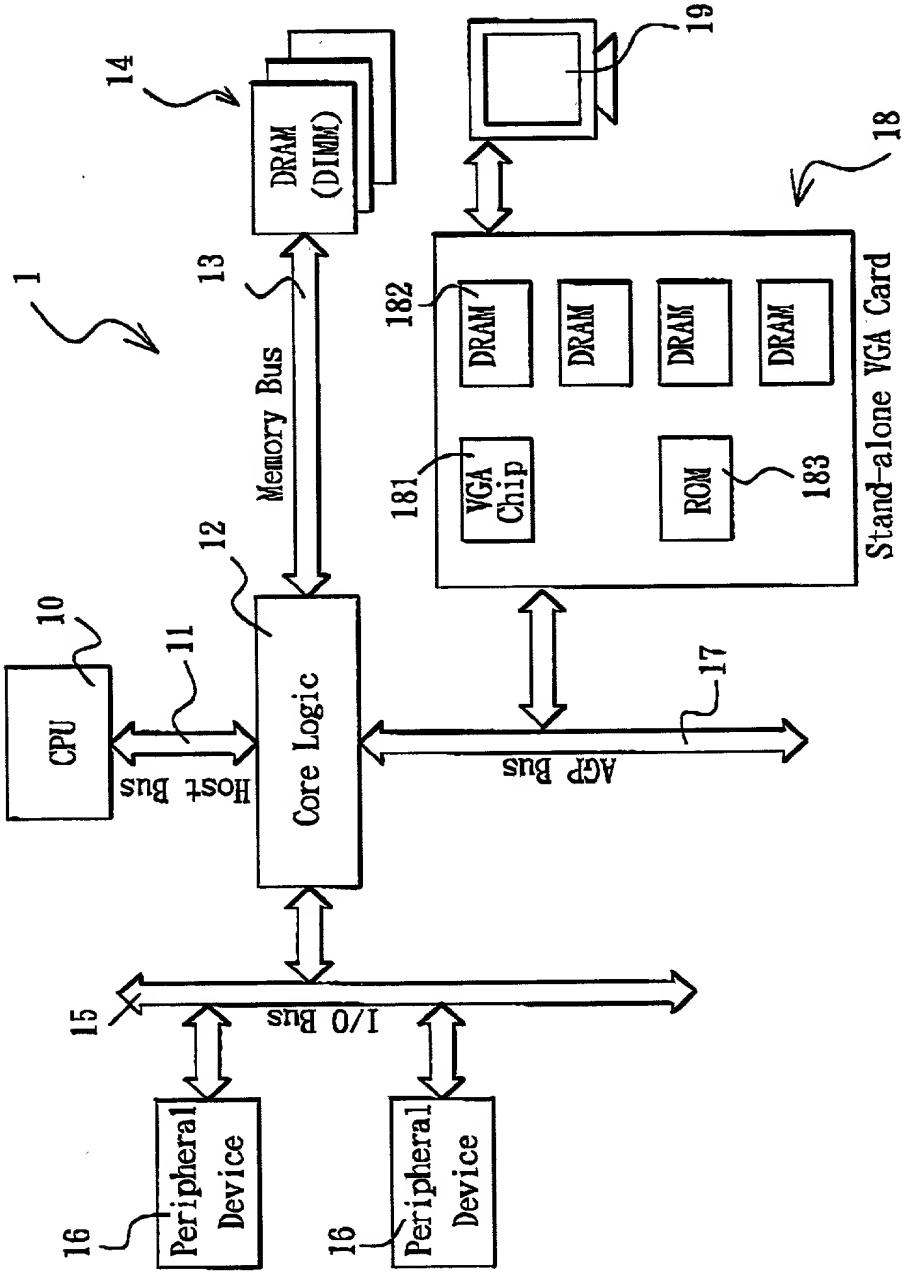

FIG. 1 PRIOR ART

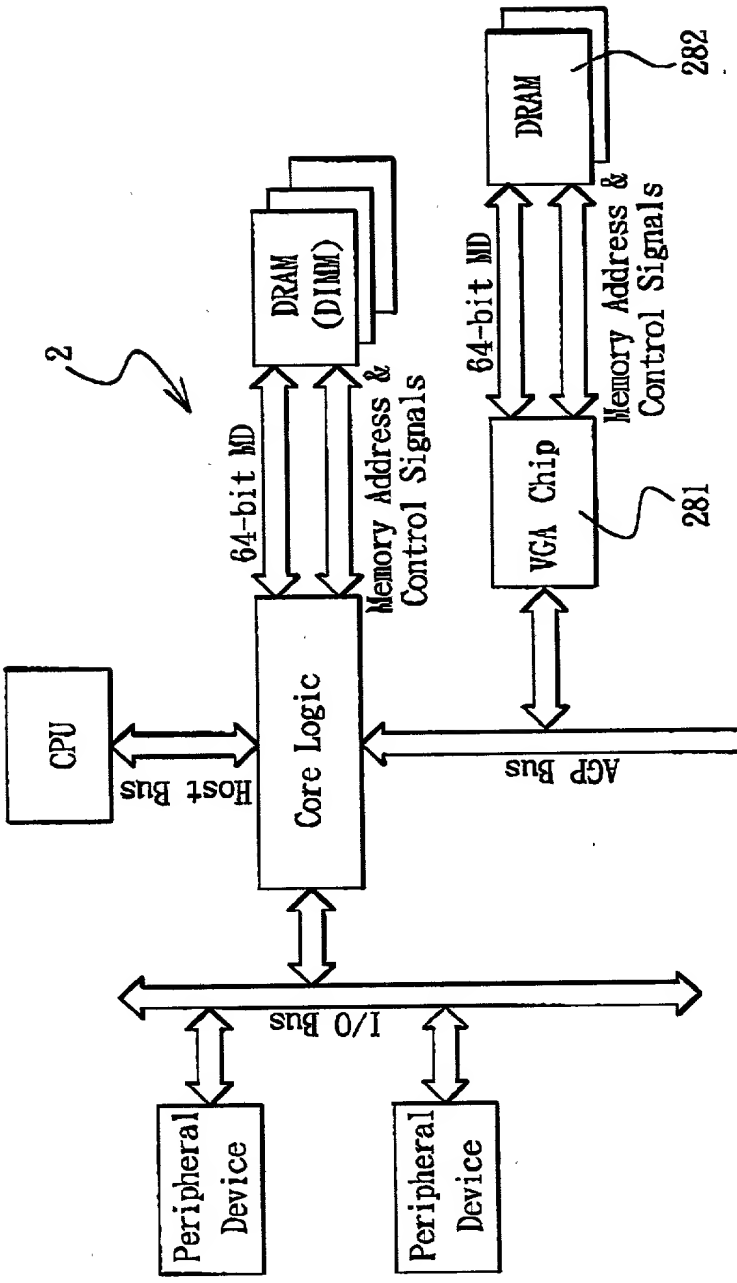

FIG. 2 PRIOR ART

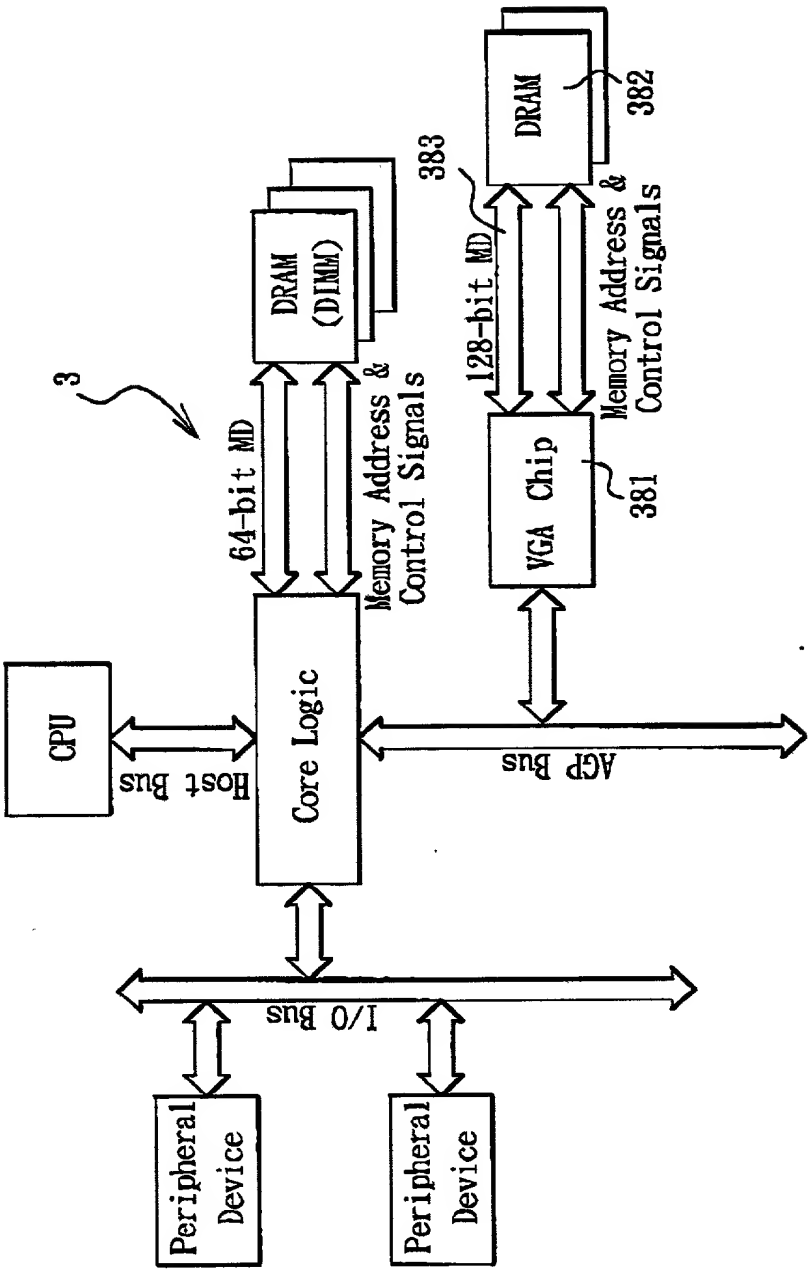
3
CPU
Host Bus
Core Logic
64-bit MD
Memory Address & Control Signals
DRAM (DIMM)
AGP Bus
VGA Chip
381
128-bit MD
383
DRAM
382
Memory Address & Control Signals
I/O Bus
Peripheral Device
Peripheral Device

FIG. 3

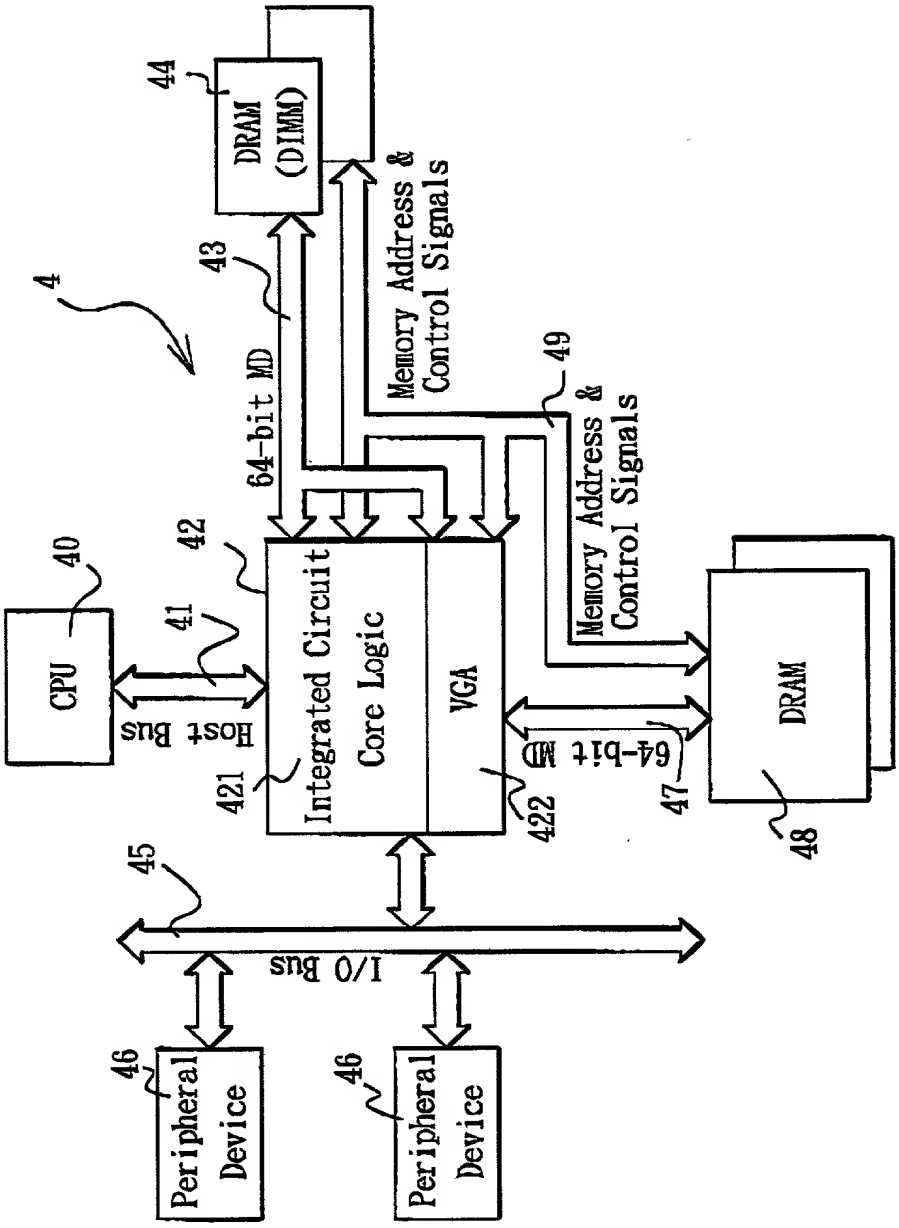
4
44
DRAM (DIMM)
43
64-bit MD
Memory Address & Control Signals
49
Memory Address & Control Signals
40
CPU
41
Host Bus
42
Integrated Circuit
Core Logic
421
VGA
422
64-bit MD
47
DRAM
48
45
I/O Bus
46
Peripheral Device
46
Peripheral Device

FIG. 4